

Appl. No. 09/446,507  
Amendment dated September 8, 2003  
Reply to Office Action of May 7, 2003

### REMARKS

Claims 1-17, 24, 26, and 32-38 are pending in this application. Claims 18-26 and 27-31 have been withdrawn from consideration to the Restriction Requirement (Paper No. 7) and now canceled without prejudice or disclaimer. Claims 1-17, 24, 26 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections while Claims 32-38 have been newly added in accordance with current Office policy, to capture the allowable features of Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

Claim 13 has been allowed without the necessity of amendment. Claims 2, 3, 6, 7, 8 and 26 have been conditionally allowed if rewritten in independent form to include all of the limitations of their respective base claims 1 and 4. The Examiner's indication of allowability of these claims is noted with appreciation. For purposes of expedition, claims 32-38 have been added to capture the subject matter of claims 2, 3, 6, 7, 8 and 26, and their respective base claims 1 and 4. As a result, claims 32-38 are believed to be in condition for allowance. As for claims 2, 3, 6, 7, 8 and 26, forbearance is respectfully requested pending Applicants' traversal of the outstanding rejection of base claims 1 and 4.

The abstract of the disclosure has been objected because it is too long and should be between 50 and 250 words. In response thereto, a new abstract is hereby submitted for the Examiner's consideration and entry.

Claims 17/14, 17/15 and 17/16 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, the Examiner asserts that claim 17 lacks proper antecedent basis for the term "said power supply circuit." The

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Examiner's assertion is well taken. Accordingly, claim 17 has been amended to overcome this rejection.

Claims 1, 4 and 5 have been rejected under 35 U.S.C. §102(b) as being anticipated by Kardontchik et al., U.S. Patent No. 5,566,204 for reasons stated on pages 2-3 of the Office Action (Paper No. 9). For purposes of expedition, base claim 1 has been amended to clarify the relationship between a phase control unit, a frequency control unit and an oscillator in a phase locked loop circuit in order to clearly distinguish over Kardontchik '204 and other prior art of record. For example, claim 1 has been amended to define "a first loop which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and a second loop which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control, wherein said first loop and said second loop are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously." These features are not disclosed or suggested in Kardontchik '204 or any other prior art references of record. As a result, the rejection of Applicants' claim 1 should be deemed moot. However, to the extent that Kardontchik '204 may still be applicable, Applicants respectfully traverse the rejection for reasons discussed herein below.

Kardontchik '204 discloses a fast acquisition clock recovery system for high speed data communications, and more specifically, an integrated CMOS circuit as shown in FIG. 2, including a receiver section with a phase-locked loop (PLL) and a transmitter section with a locked loop (LL), wherein the receiver section provides fast clock acquisition of an incoming data signal. As shown in FIG. 1, the switching

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between phase information and frequency information is handled by using the MUX 56 in response to the TRANSITION DETECTOR signal 58. In other words, Kardontchik '204 discloses a clock recovery scheme utilizing an ordinary timing extraction PLL operation for transceivers in which frequency is made coincident first and then phase is made coincident, but not controlling both phase and frequency continuously.

In contrast to Kardontchik '204, Applicants' base claim 1, as amended, defines a phase locked loop (PLL) suitable for use on clock regeneration for microcomputers, though not limited thereto, which operates such that both the phase control loop and the frequency control loop are always connected and are operating continuously. The frequency control is realized by using F/I conversion to linearize the VCO/CCO characteristic, to thereby realize a wide range operation.

The phase control loop and the frequency control loop are always connected for continuous operation, as shown in FIG. 1 and described on page 13, lines 19-24 of Applicants' specification. For example, on page 13, lines 19-24, Applicants describe that "the proportional controller 3000 first causes the output signal Sv of oscillator 100 to be synchronized in frequency with the input signal Sin; then, the integral controller 2000 lets the output signal Sv be synchronized in phase with input signal Sin."

The rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim.

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Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989);  
Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed.  
Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051  
(Fed. Cir. 1987). The corollary of that rule is that absence from the reference of  
any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc.,  
793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

In the present situation, since Kardontchik '204 fails to disclose or suggest the  
relationship between "a first loop" and "a second loop" wherein both "said first loop  
and said second loop are connected to said oscillator at all times so as to carry out  
the integral control and the proportional control continuously" as expressly defined in  
Applicants' claim 1, Applicants respectfully request that the rejection of claim 1 and  
its dependent claims 4-5 be withdrawn.

Separately, claim 14 has been rejected under 35 U.S.C. §102(e) as being  
anticipated by Barrett et al., U.S. Patent No. 5,422,911 for reasons stated on pages  
3-4 of the Office Action (Paper No. 9). Again, for purposes of expedition, base claim  
14 has been amended to clarify the relationship between an information processing  
apparatus for data processing based on a clock frequency and a circuitry connected  
to the information processing apparatus for enabling the information processing  
apparatus to render variable "a clock frequency based on a remaining charge of a  
battery so that said information processing apparatus operates on a frequency  
commensurate which the remaining charge of said battery." This feature is **not**  
disclosed or suggested in Barrett '911 or any other prior art references of record. As  
a result, the rejection of Applicants' claim 14 should be deemed moot. However, to

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the extent that Barrett '911 may still be applicable, Applicants respectfully traverse the rejection for reasons discussed herein below.

Barrett '911 discloses a selective call receiver, as shown in FIG. 1, using a phase lock loop (PLL) frequency synthesizer provided with a number of components, shown in FIG. 4, including a charge pump phase/frequency detector 403, a N counter 404, a voltage-to-current converter 410, a programmable gain current multiplier 412, and a current control variable frequency oscillator 413. According to Barrett '911, N is set in control multiplier 412 and N counter 404 by means of the frequency control signal code from controller so that the frequency signal may be changed programmably. To this end, the oscillation frequency of the internal oscillator 414 in the PLL is changed so as to enable a wide range operation.

In contrast to the PLL of Barrett '911, Applicants' claim 14 defines a crystal oscillation frequency, based on the battery residue or the remaining charge on the battery, which is frequency-divided so that the reference frequency may be lowered to thereby realize an operating frequency commensurate with the battery residue or the remaining charge in the battery.

Again, since the subject matter of Applicants' base claim 14 and that of Barrett '991 are completely different, Applicants respectfully submit that Barrett '911 does not anticipate Applicants' claim 14 and request that the rejection of Applicants' claim 14 be withdrawn.

Claim 24 has been rejected under 35 U.S.C. §103 as being unpatentable over Alvarez et al., U.S. Patent No. 5,362,990 for reasons stated on page 3 of the Office Action (Paper No. 9). However, Applicants respectfully submit that features of Applicants' claim 24 are not disclosed or suggested by Alvarez '990, whether taken

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individually or in combination with any other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection for the following reasons.

Claim 24 defines a phase locked loop circuit comprising:

**a phase comparator circuit** for outputting a phase difference signal from anyone of two output terminals in accordance with a phase difference between two signals as input thereto;

**a charge pump circuit** responsive to receipt of the phase difference signal from said phase comparator circuit for permitting charging and discharging of a capacitor to generate a control voltage signal; and

**an oscillator** responsive to the control voltage signal from said charge pump circuit for adjusting a transmission frequency,

wherein said charge pump circuit includes a first current switch circuit for charging up said capacitor in deference to the phase difference signal as output from one output terminal of said phase comparator circuit, and a second current switch circuit for discharging said capacitor in response to the phase difference signal as output from a remaining one of the output terminals of said phase comparator circuit, and

wherein said first and second current switch circuits comprise a current switch using a CMOS inverter with a control electrode forward-biased and a complementary paired output voltage switch for driving said current switch with an output connected to a low voltage-side electrode of said current switch.

In contrast to Applicants' claim 24, Alvarez '990 simply discloses a charge pump with a programmable pump current. As shown in FIG. 1, MOS 63 and MOS 68 are used as switches to turn on/off constant current MOS(s) 60 and 68 with Up and DOWN signals applied to the gates of the switch MOS(s) 62 and 63, respectively. However, the source side of the constant current MOS 60 or 66 assumes a high impedance (the source side is in open state having no signal source. The source side becomes at VCC or ground potential when the switch MOS is "on"), when the switches transit from "on" to "off". Due to such a configuration,

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transition settlement time is long due to parasitic capacitance of the MOS switch, making it impossible to realize a precision fast switch.

In contrast to Alvarez '990, Applicants' claim 14 utilizes a CMOS inverter as a switch so that the source side of the constant current MOS is connected to power supply voltage VCC or ground potential GND in order to always provide a low impedance. By virtue of this arrangement, the transition settling time due to switch's parasitic capacitance is short in both "on" and "off", making it possible to achieve a high precision (1 to 2 %) and fast operation (20 ps, GHz operation).

In order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, the Examiner must show that the prior art reference (or references when combined) must teach or suggest all the claim limitations, and that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings, provided with a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143.

In the present situation, Alvarez '990 fails to disclose and suggest novel features of Applicants' claim 24. Therefore, Applicants respectfully request that the rejection of claim 24 be withdrawn.

Lastly, claims 9, 10, 11, 12, 15 and 16 have been rejected under 35 U.S.C. §103 as being unpatentable over Barrett '991, in view of Kardontchik '204 for reasons stated on page 4 of the Office Action (Paper No. 9). Again, Applicants

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submit that features of Applicants' claims 9, 10, 11, 12, 15 and 16 are not disclosed or suggested by Barrett '911 and Kardontchik '204, whether taken individually or in combination with any other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection for the following reasons.

First of all, Applicants note that claims 15-16 depend upon base claim 14, which Applicants have already pointed as patentably distinguishable over Barrett '911 for reasons discussed. As dependent claims, claims 15-16 should be allowed if base claim 14 is allowable.

With regard to claim 9, claim 9 defines an information processing apparatus as comprising:

- a clock generator unit including a first control signal generator unit for generation of a first control signal based on a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal based on a difference in frequency between an input signal and an output signal, and an oscillator for generation of a clock signal based on said first control signal and said second control signal;

- a clock control unit for controlling the clock signal as output from said clock generator unit; and

- a logic unit for processing data based on the clock signal as generated by said clock generator unit.

Likewise, claim 11 alternatively defines an information processing apparatus as comprising:

- a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input thereto;

- a clock control unit for controlling said first clock signal as input to said clock generator unit; and

- a logic unit for processing data on the basis of said second clock signal.



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As expressly defined in each of Applicants' base claims 9 and 11, the phase locked loop (PLL) circuit is provided with two loops (i.e., first feedback circuit and second feedback circuit) operating continuously.

In contrast to Applicants' base claims 9 and 11, Barrett '911, as a primary reference, only discloses a selective call receiver, as shown in FIG. 1, using a phase lock loop (PLL) frequency synthesizer provided with a number of components, shown in FIG. 4, including a charge pump phase/frequency detector 403, a N counter 404, a voltage-to-current converter 410, a programmable gain current multiplier 412, and a current control variable frequency oscillator 413. Again, Barrett '911 changes the oscillation frequency of an internal oscillator 414 so as to enable a wide range operation. However, no disclosure of any "clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input thereto" as defined in Applicants' base claim 11 and any "clock generator unit including a first control signal generator unit for generation of a first control signal based on a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal based on a difference in frequency between an input signal and an output signal, and an oscillator for generation of a clock signal based on said first control signal and said second control signal" as defined in Applicants' base claim 9.

As a secondary reference, Kardontchik '204 does not remedy the noted deficiencies of Barrett '911 in order to arrive at Applicants' base claims 9 and 11.

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This is because Kardontchik '204 only discloses an integrated CMOS circuit as shown in FIG. 2, including a receiver section with a phase-locked loop (PLL) and a transmitter section with a locked loop (LL), wherein the receiver section provides fast clock acquisition of an incoming data signal.

Neither Barrett '911 nor Kardontchik '204 discloses any clock generator unit having two loops operating continuously. In fact, in Kardontchik '204, the phase detector and frequency divider are provided and switched by the multiplexer so that only one of them is operating at a time. Likewise, in Barrett '911, the phase/frequency detector 403 is made up of an integrated single circuitry having a single loop.

In view of the foregoing deficiencies of the proposed combination of Barrett '911 and Kardontchik 204, Applicants respectfully request that the rejection of claims 9, 10, 11, 12, 15 and 16 be withdrawn.

Lastly, claims 33-38, as previously discussed, have been newly added to alternatively define Applicants' disclosed invention over the prior art of record. These claims are allowable because they define the subject matter of allowed claims 2, 3, 6, 7, 8 and 26. Claims 33-38, as newly added, replace the canceled claims 18-23, 25 and 27-32 (withdrawn due to the Restriction Requirement). A fee of \$168.00 is incurred by the addition of two (2) extra independent claims.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

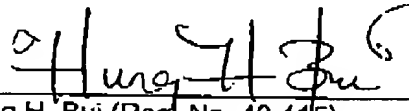
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To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 500.38017X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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